

Model Name: GA-H81M-S2PV

Revision 3.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1150-A
05	CPU LGA1150-B
06	CPU LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH FDI,DMI,USB,PCIE,NVRAM
10	PCH DP,CLK BUFFER
11	PCH HOST,SATA,PCI
12	PCH GPIO,CTRL,AUDIO
13	PCH PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS X1 SLOT
16	PCI SLOT 1,2
17	ITE 8620 LPC IO
18	COM,LPT,KB MS
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	R USB30,FP,FUSB,SPK,SATALED
22	Realtek ALC887-VD2
23	REAR AUDIO JACK
24	REALTEK RTL8111G
25	DISCRETE POWER
26	ATX
27	VCORE ISL95812 1

SHEET

TITLE

28	VCORE ISL95812 2
29	RT8120 DDR POWER
31	DVI
32	IT8892E

Gigabyte Technology

Cover Sheet		
Size Custom	Document Number GA-H81M-S2PV	Rev 3.0
Date: Thursday, August 07, 2014	Sheet 1	of 31

Revision 3.0

Component value change history

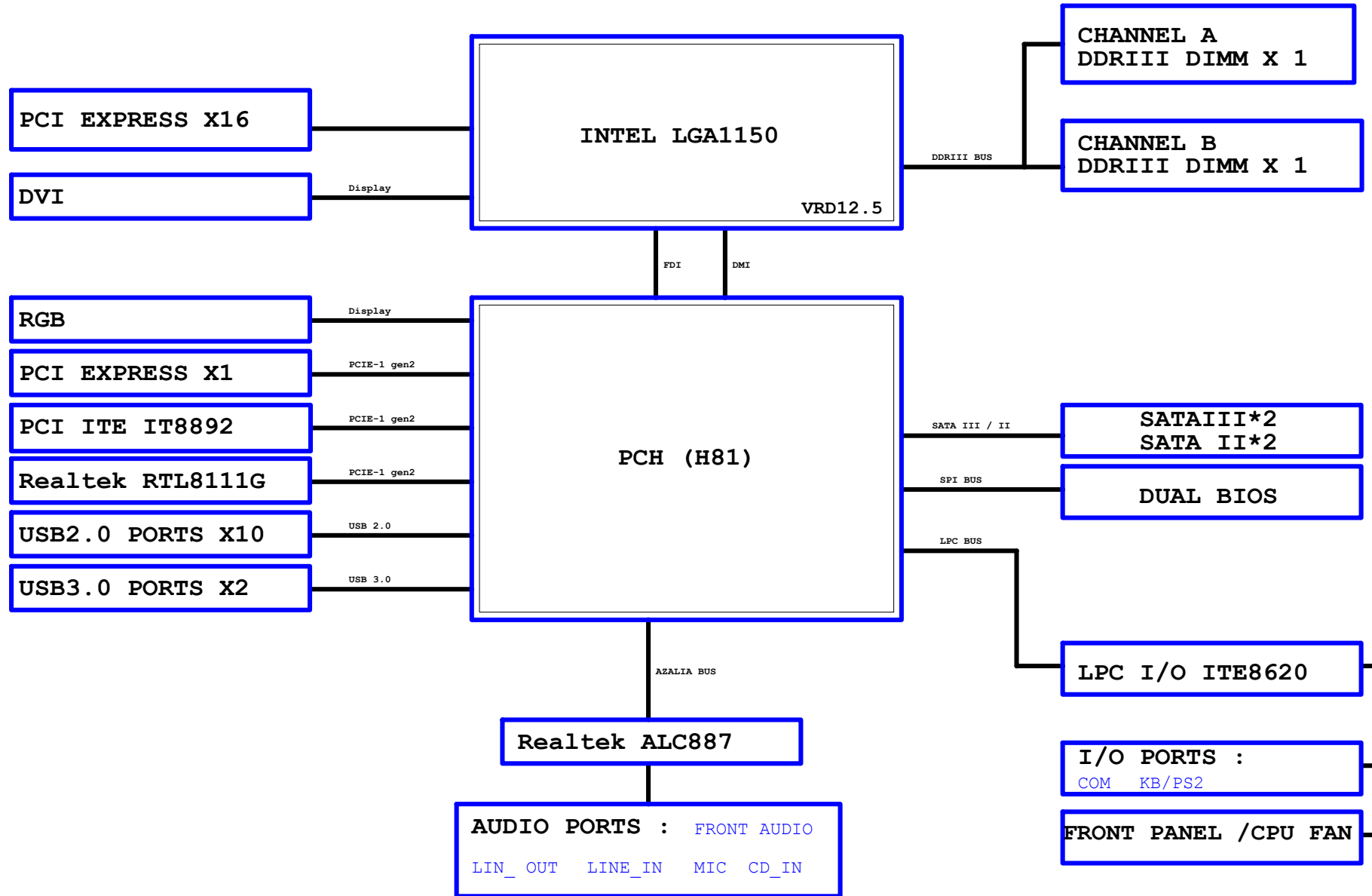
2014/07/31

Data	Change Item	Reason
2013/06/24	Update Rev to 1.0	PBOM: 9MH81MS2V-00-10A
2013/06/28	Update Rev to 1.01	PBOM: 9MH81MS2V-00-10B
	ADD RSMRST DELAY	
	ADD 5VSB Protection	
2013/07/03	Remove Super I/O OVP/UVF Function	PBOM: 9MH81MS2V-00-10C
2013/07/11	導入5VSB OVP Protection	PBOM: 9MH81MS2V-00-10D
	DEL R704: 8.2K/4	
	ADD R706: 8.2K/4	
	R705: 715/4/1 -> 825/4/1	
	AUDIO AZ2225-01L CD1移除	
2013/08/19	REMOVE WR57 FIX IT8620 TEMP ISSUE	FPBOM: 9MH81MS2V-00-10E
2013/09/13	Update to R1.02	
	Follow Crystal Trace Rule	
	SYS_FAN, DDR 0ohm 0402 -> 0603	
	Update Fuse 1206 Footprint "POLYSWITCH-1206-1"	
	Update PPAK Footprint "Q_TDS0N8-GDS-T"	
2013/10/22	NX1: 25M/20p -> 12p	FPBOM: 9MH81MS2V-00-10F
	NC7, NX8: 27p -> 10p	
2013/11/04	NC7, NX8: 10p -> 15p	FPBOM: 9MH81MS2V-00-10H
2013/11/19	R1.03	FPBOM: 9MH81MS2V-00-10G (R1.03)
	FIX Crystal 2G phone issue	
2013/11/27	MR17 0ohm -> 0603 FUSE(10FP5-06100B-00R)	FPBOM: 9MH81MS2V-00-10I (R1.03)
2014/02/17	Sales Costdown Rev	
	CPU Power ISL95812 1U2D -> ISL95812 1U1D	
	DVI Non-Level Shift	
	BIOS Size 64M -> 32M	
	0ohm -> Short Pad	
2014/02/25	整合電阻成排阻	
2014/04/02	ADD NC60, NC61	FPBOM: 9MH81MS2V-00-20A
	DEL OR47, OC27, RS2	

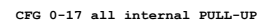
Circuit or PCB layout change

[illegible]

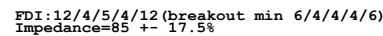
BLOCK DIAGRAM



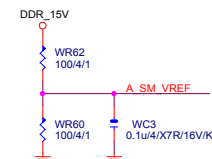
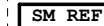
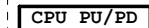
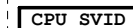
(E)



(D)



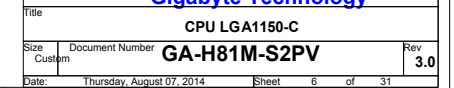
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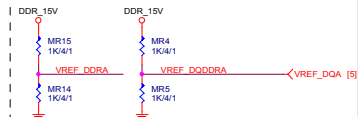
LGA1150

(A)

LGA1150A			
MAAA0	AU13	DDR0_MA0	DDR0_D00
MAAA1	AV16	DDR0_MA1	DDR0_D01
MAAA2	AU16	DDR0_MA2	DDR0_D02
MAAA3	AW17	DDR0_MA3	DDR0_D03
MAAA4	AU17	DDR0_MA4	DDR0_D04
MAAA5	AW18	DDR0_MA5	DDR0_D05
MAAA6	AW17	DDR0_MA6	DDR0_D06
MAAA7	AT18	DDR0_MA7	DDR0_D07
MAAA8	AU18	DDR0_MA8	DDR0_D08
MAAA9	AT19	DDR0_MA9	DDR0_D09
MAAA10	AW11	DDR0_MA10	DDR0_D10
MAAA11	AV19	DDR0_MA11	DDR0_D11
MAAA12	AU19	DDR0_MA12	DDR0_D12
MAAA13	AY10	DDR0_MA13	DDR0_D13
MAAA14	AT20	DDR0_MA14	DDR0_D14
MAAA15	AU21	DDR0_MA15	DDR0_D15
MODT_A0	AW10	DDR0_ODT0	DDR0_D16
MODT_A1	AY3	DDR0_ODT1	DDR0_D17
	AW9	DDR0_ODT2	DDR0_D18
	AW8	DDR0_ODT3	DDR0_D19
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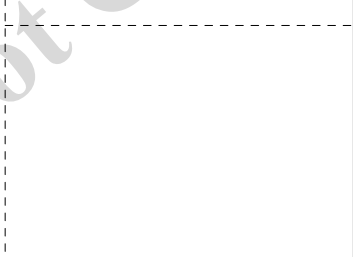
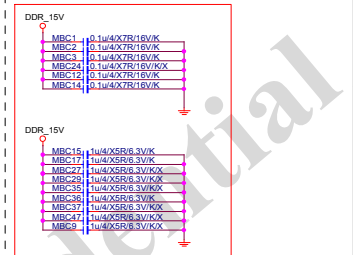


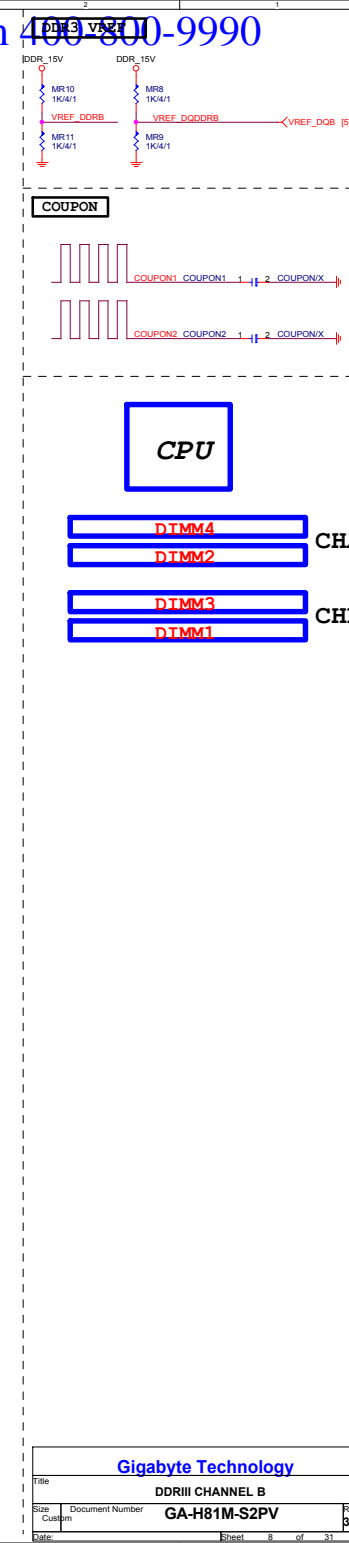
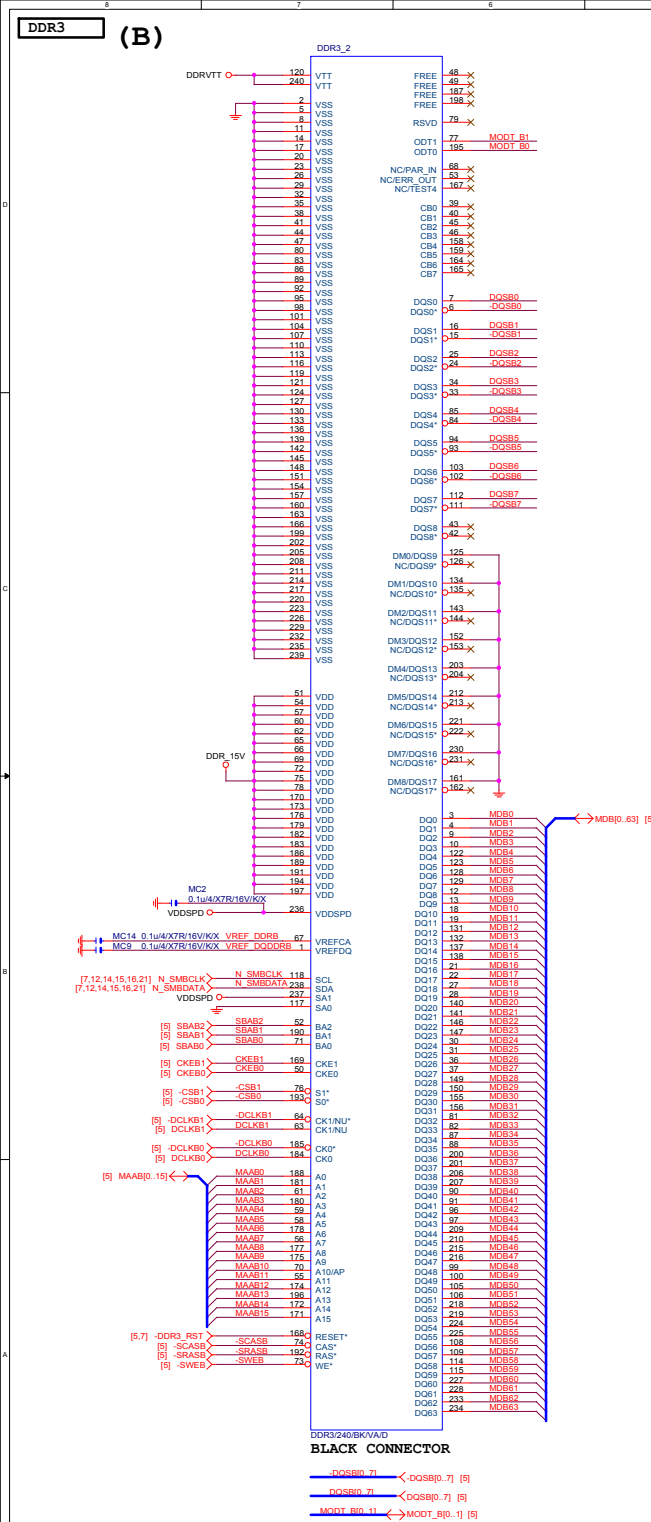
DDR3



DDR_15V

MEC1
560uF/FP/D/6.3V/69A/11mV[11CO2-695600-09R]
MEC2
560uF/FP/D/6.3V/69A/11mV[11CO2-695600-09R]

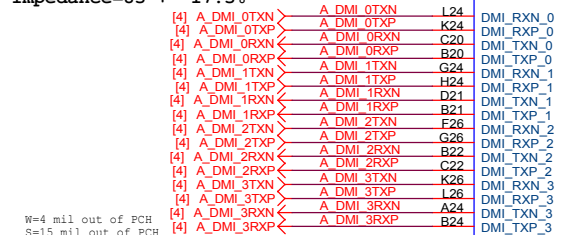




PCH

(B)

DMI:12/4/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +/- 17.5%



PCIE Only

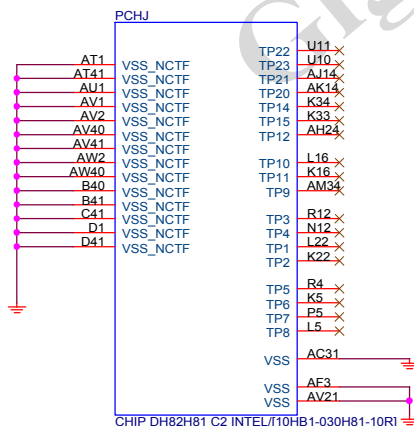
N/A

放靠近 Device & PCI-E Slot
Impedance=80 +/- 17.5%

PCIE1:16/5/5/5/16 (breakout min 8/4/4/4/8)

PCH

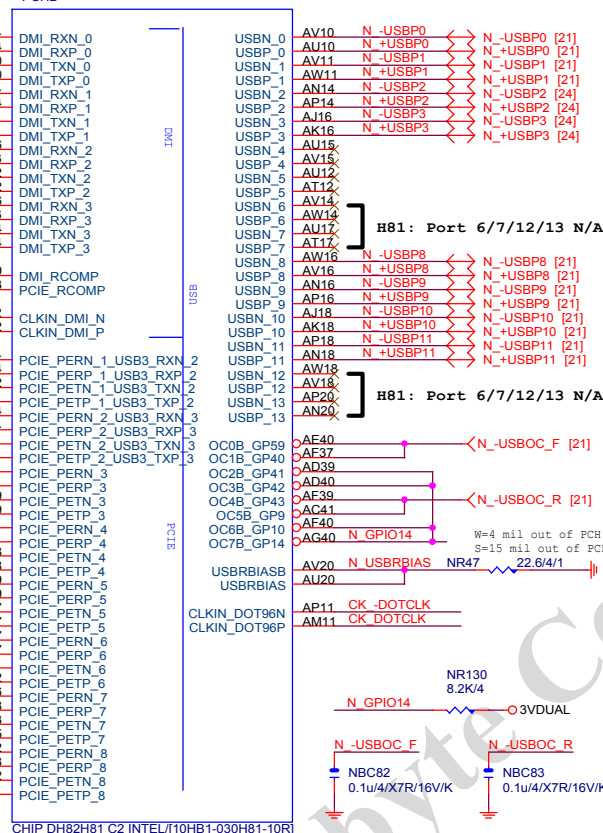
(J)



CHIP DH82H81 C2 INTEL(10HB1-030H81-10R)

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +/- 17.5%

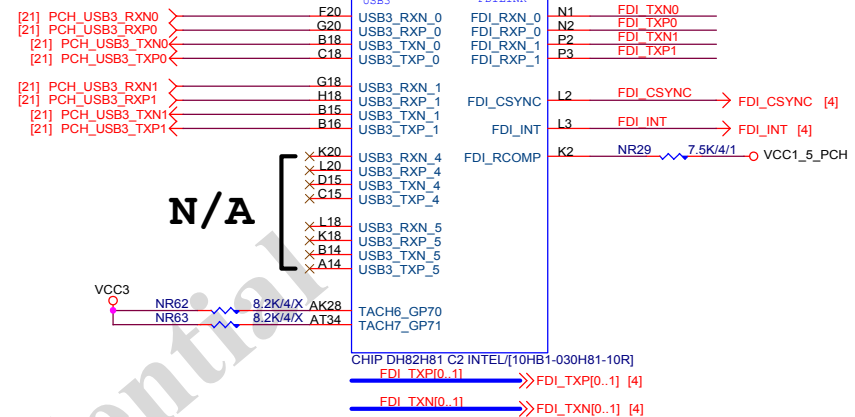
PCHB



CHIP DH82H81 C2 INTEL(10HB1-030H81-10R)

PCH

(F)



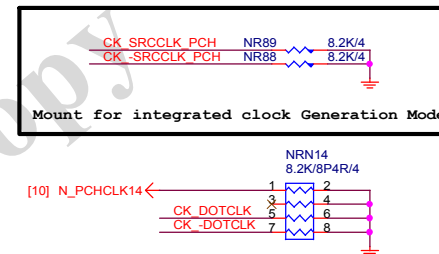
CHIP DH82H81 C2 INTEL(10HB1-030H81-10R)

FDI_TXP0_11 >>> FDI_TXP0[0..1] [4]

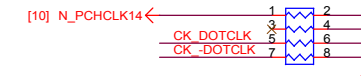
FDI_TXN0_11 >>> FDI_TXN0[0..1] [4]

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +/- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

PCH CLK PD



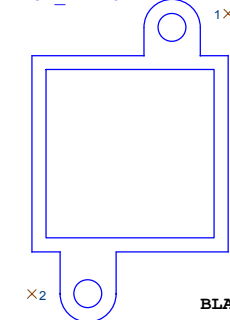
Mount for integrated clock Generation Mode



PCH H/S

LOW COST ICH7 HEATSINK

SB_HEATSINK



PCH_HS
PCH_HS(12SP2-030005-51R_12SP2-030005-52R_12SP2-030005-53R)

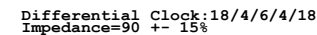
USB TABLE

OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

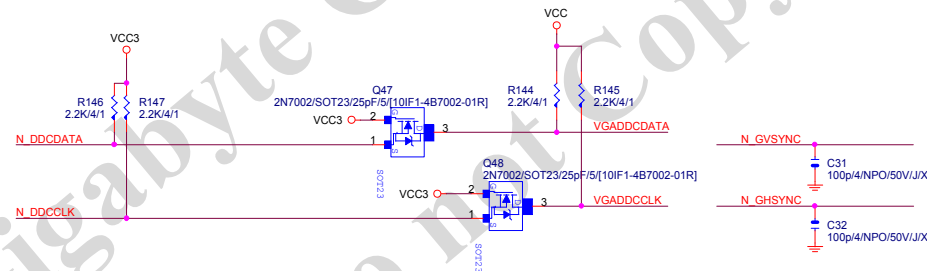
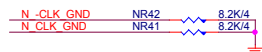
USB OC#	Configure
OC0#	R_USB30
OC1#	USB_LAN
OC2#	N/A
OC3#	N/A
OC4#	F_USB1
OC5#	F_USB2
OC6#	N/A
OC7#	Not Use

Gigabyte Technology

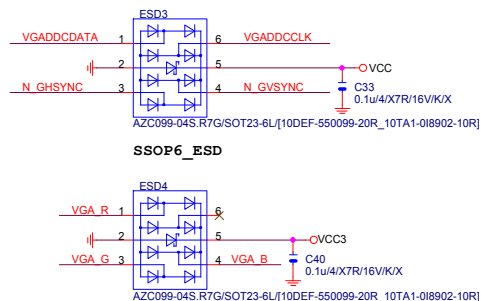
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Size	Document Number	GA-H81M-S2PV	
Custom		Rev 3.0	
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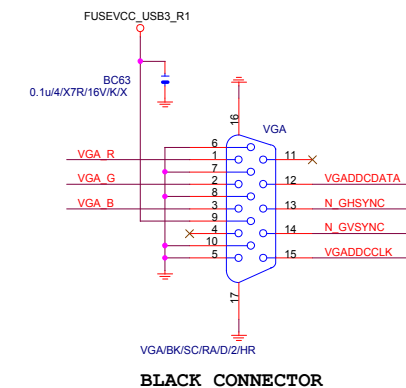
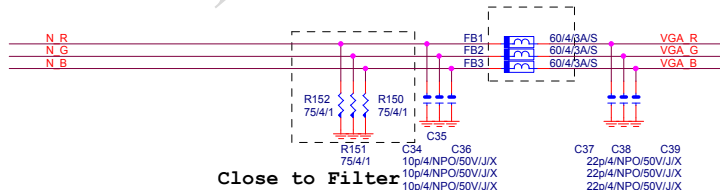
VGA CONNECTOR



VGA ESD

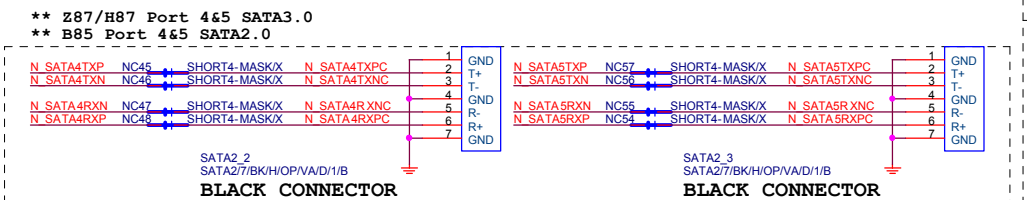
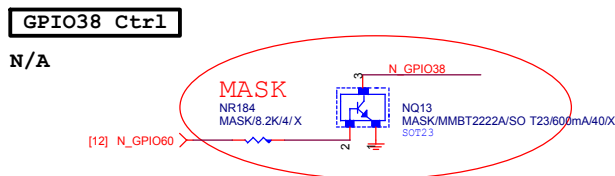
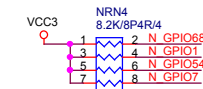
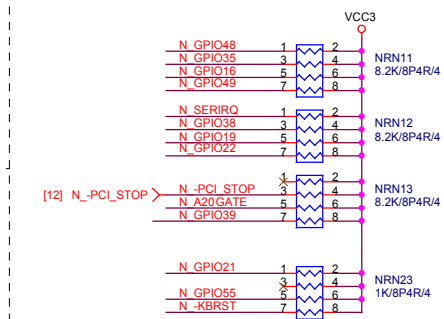
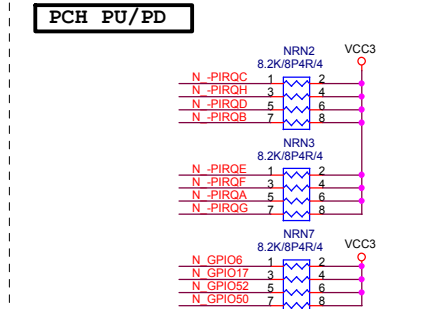
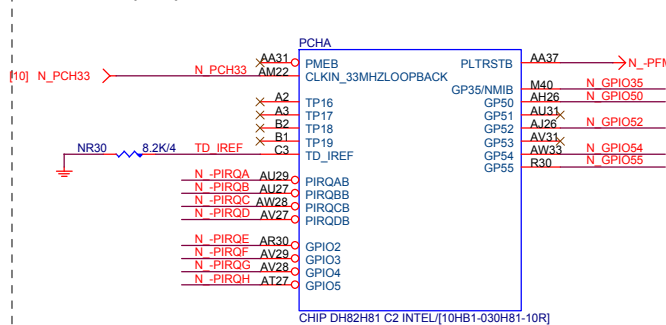


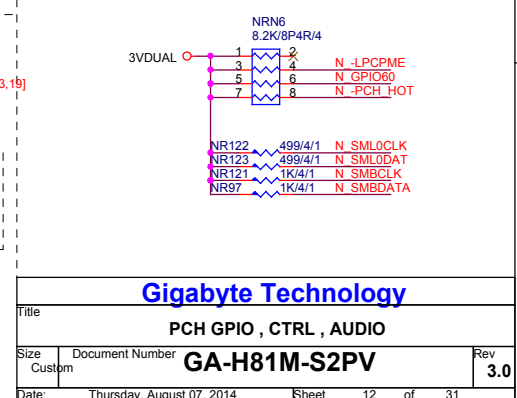
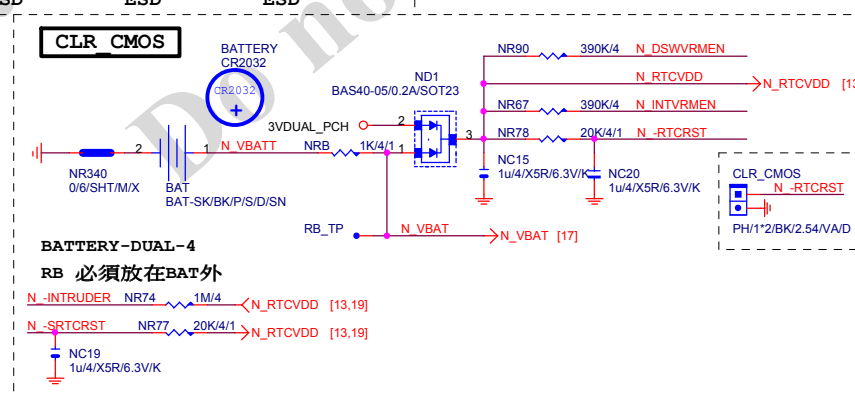
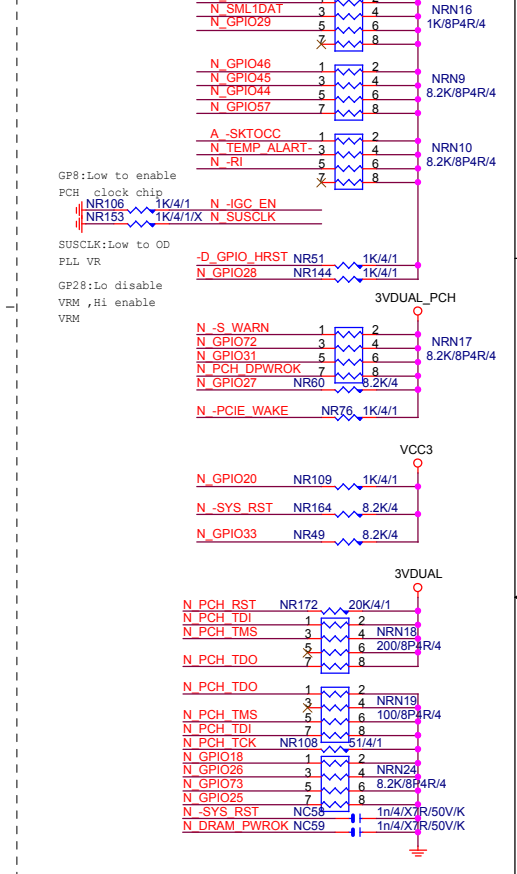
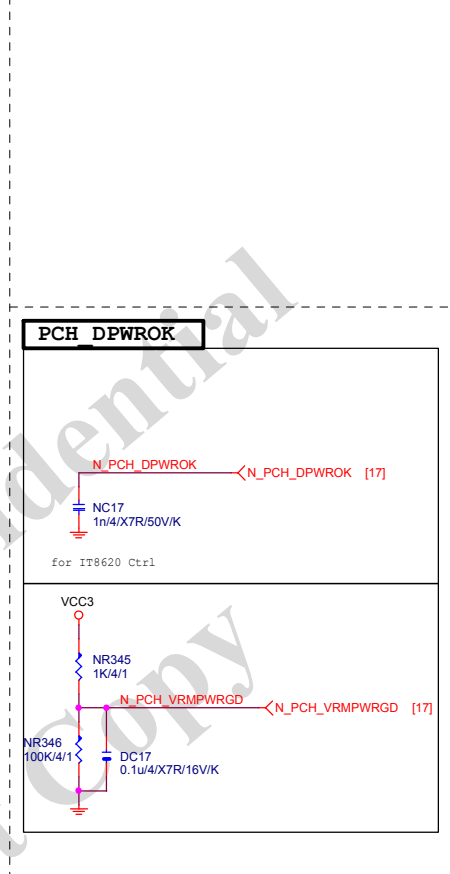
VGA DDC



Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number		Rev
Custom	GA-H81M-S2PV		3.0
Date:	Thursday, August 07, 2014	Sheet	10 of 31



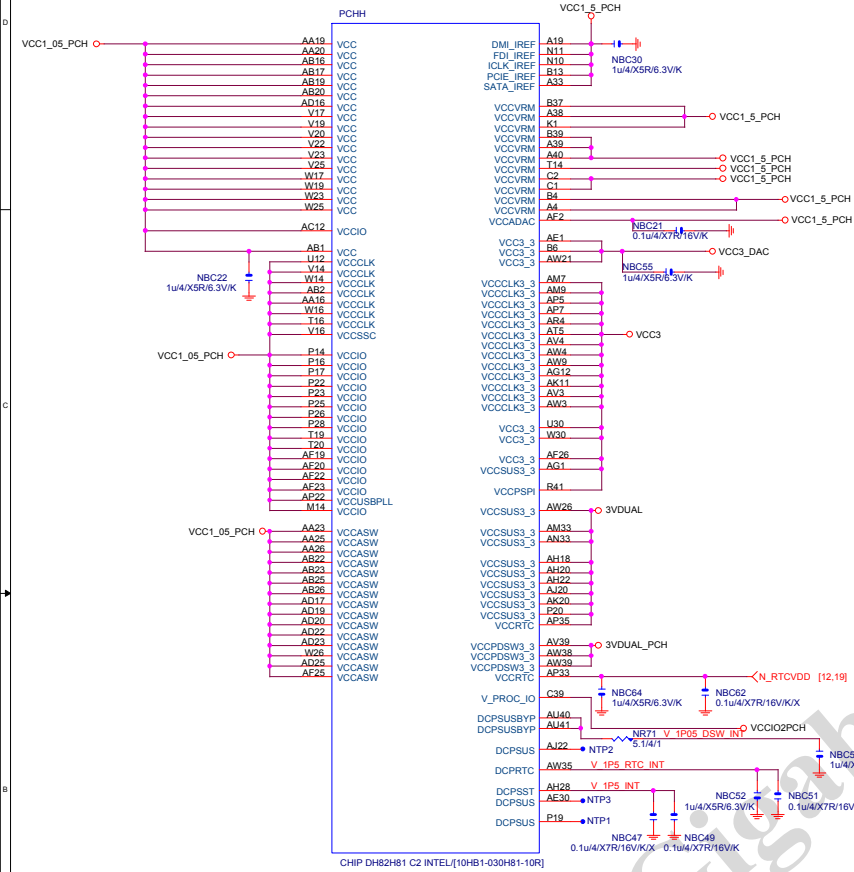


PCH (H)

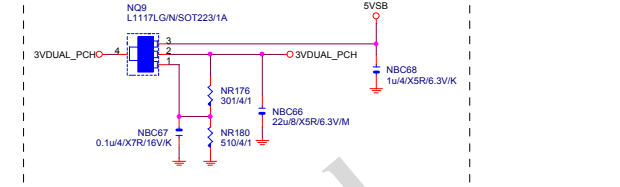
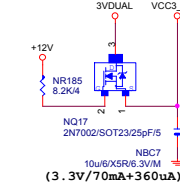
VCC3_DAC

3VDUAL_PCH

SHT_PWR

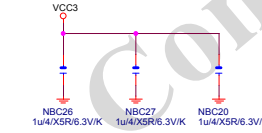


CLOSE北橋(注意震盪水波紋)

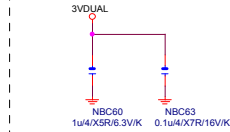
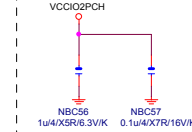


CAP

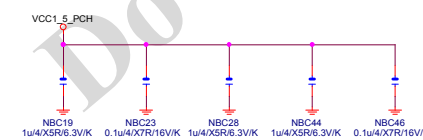
(3.3V) (X6)



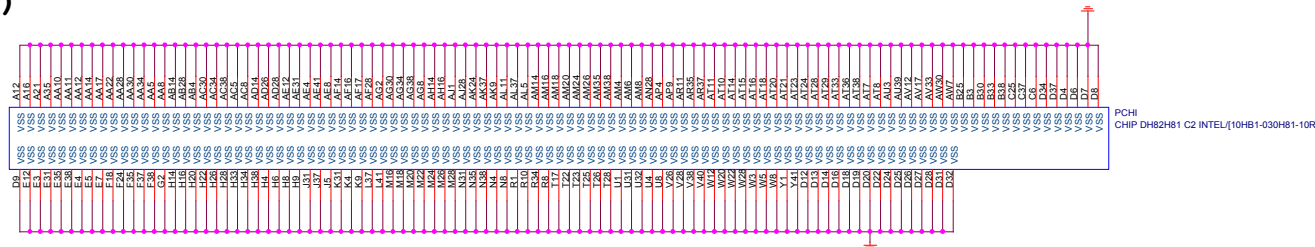
(1.05V)(X2) (3.3V) (X2)



(1.5V) (X5)

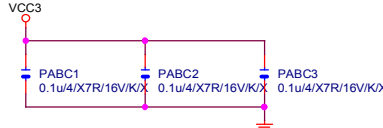


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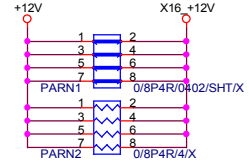


PCIEX16 CAP

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PCIEX16 PROTECT SHT



PCIEX16 AC CAP

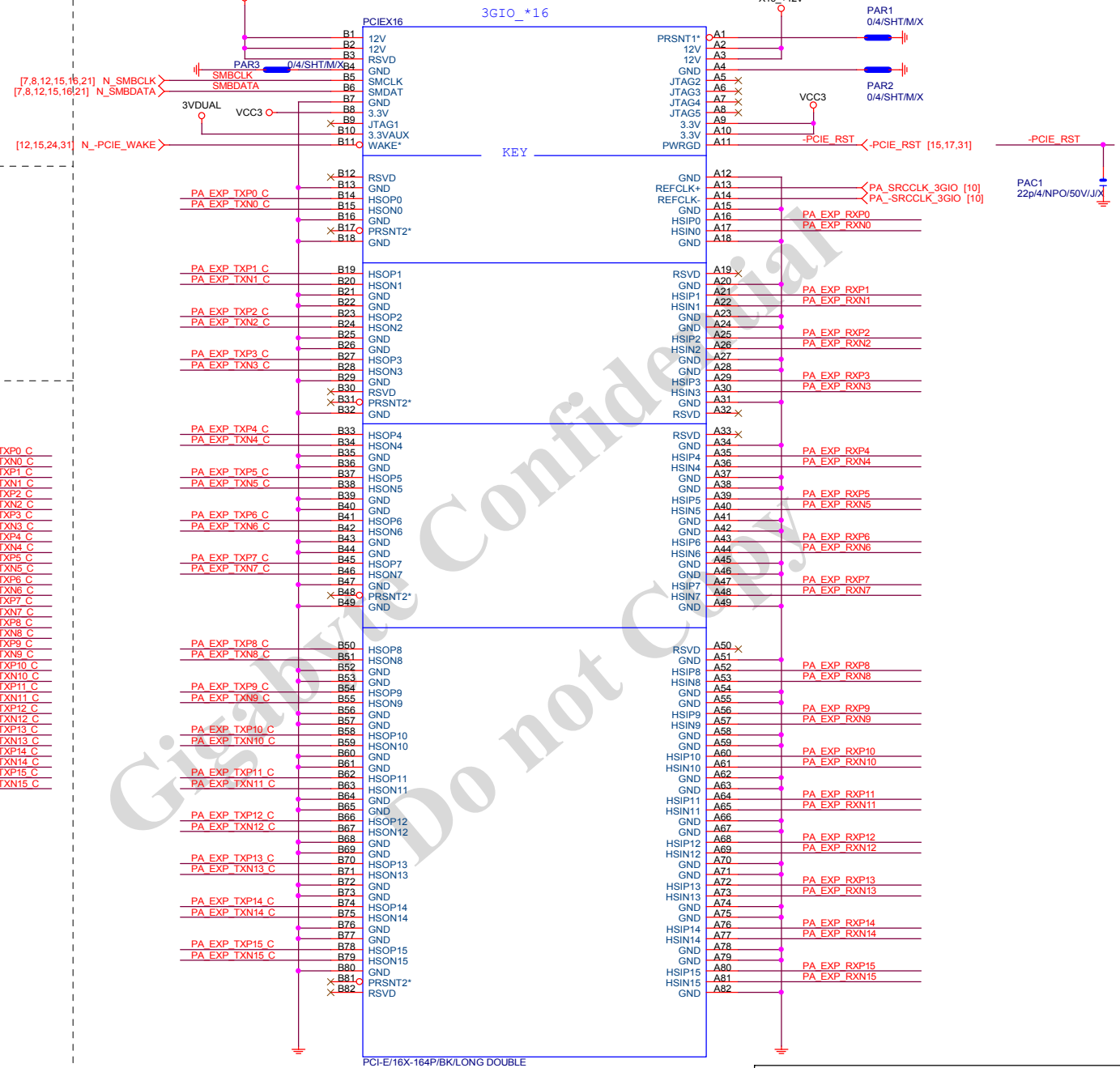
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PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
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PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
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PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXP0_15] >>>PA_EXP_RXP[0..15] [4]
 PA EXP RXN0_15] >>>PA_EXP_RXN[0..15] [4]
 PA EXP TXP0_15] >>>PA_EXP_TXP[0..15] [4]
 PA EXP TXN0_15] >>>PA_EXP_TXN[0..15] [4]

PCIEX16 SLOT

www.xinxunwei.com 400-800-9990

PCIESLOT-164DN-Q-1



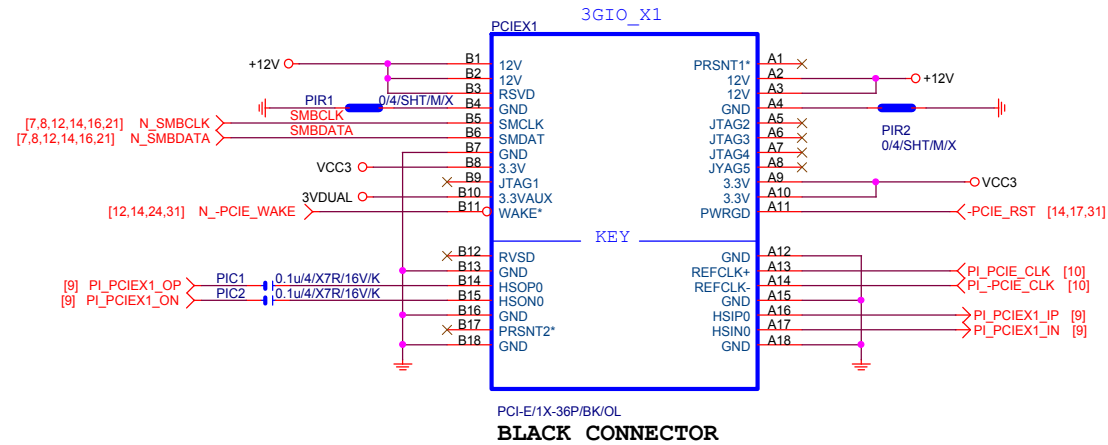
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BLACK CONNECTOR

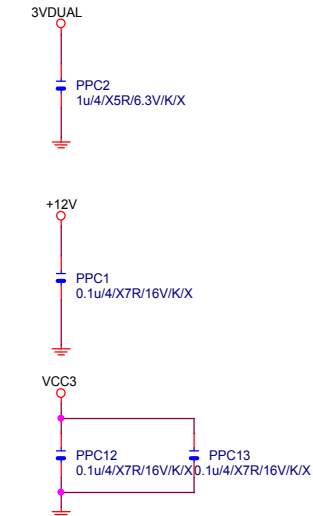
Gigabyte Technology

Title			PCI EXPRESS * 16		
Size	Document Number	Rev			
Custom	GA-H81M-S2PV	3.0			
Date:	Thursday, August 07, 2014	Sheet	14	of	31

PCIEX1 SLOT

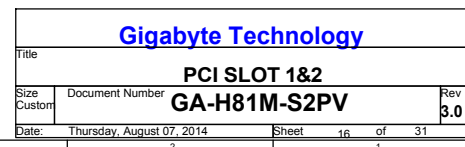
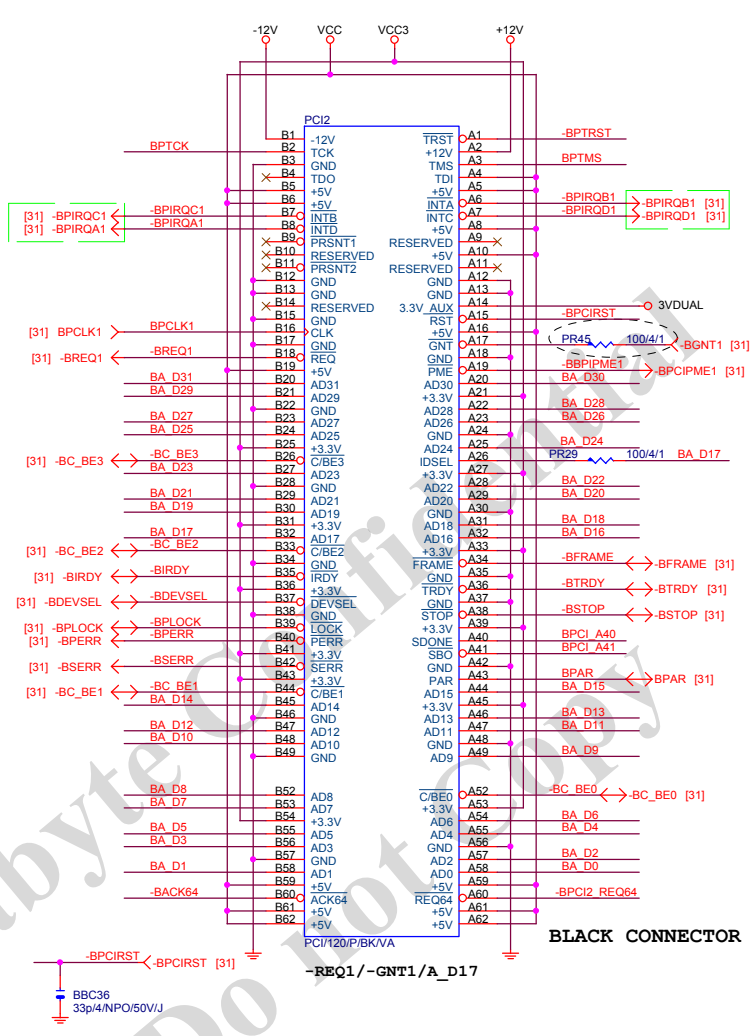


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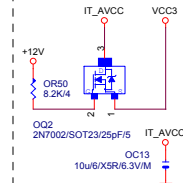
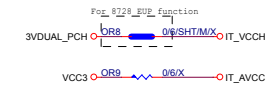
Gigabyte Technology

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Size	Document Number	GA-H81M-S2PV	
Custom		Rev 3.0	
Date:	Thursday, August 07, 2014	Sheet 15	of 31

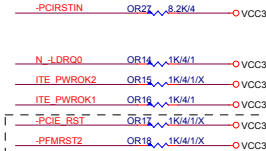


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PWR SHT

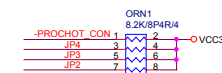


SIO	PU
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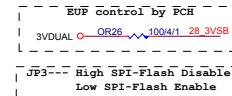


DO8 : N/A

SIO STRAP



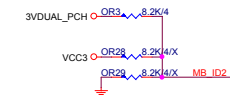
ITE recommand



Power leakage



MB ID

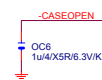


SIO CAP

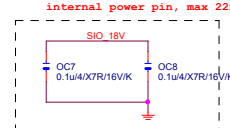
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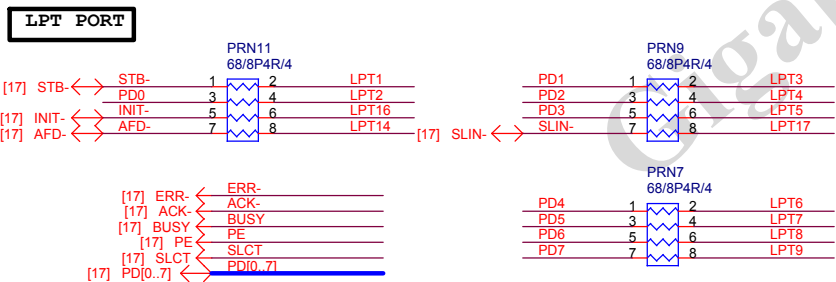
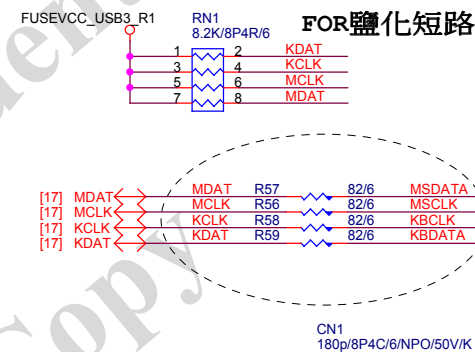
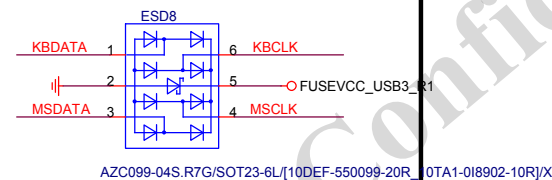
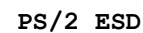
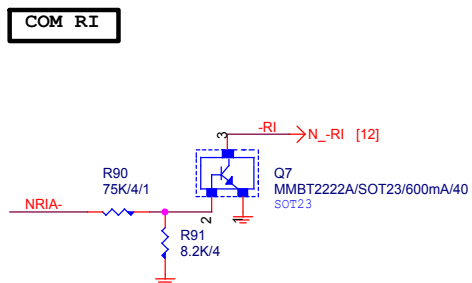
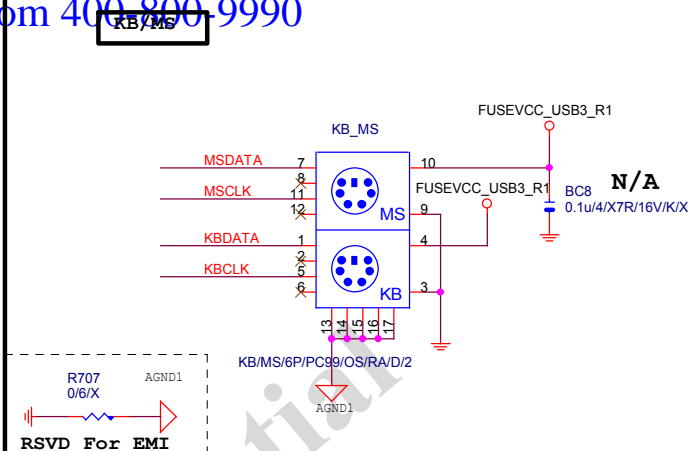
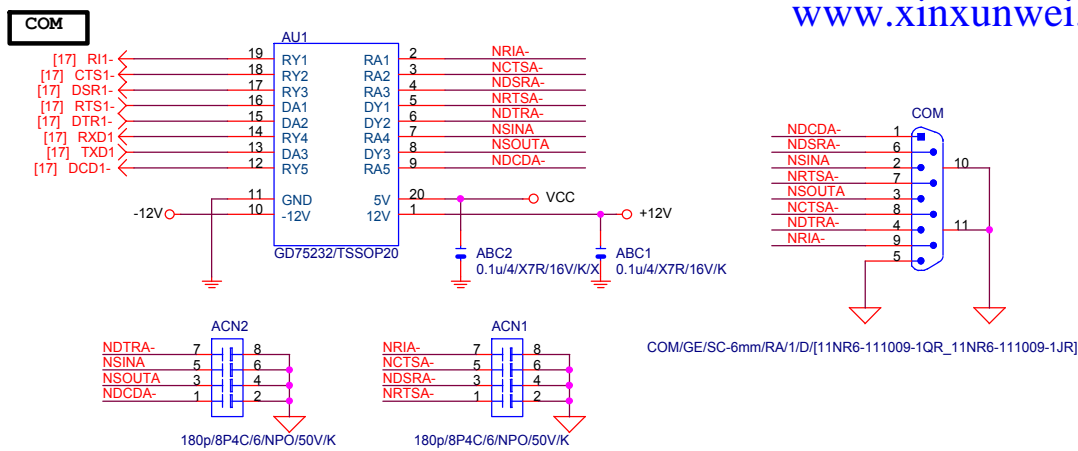
DUAL BIOS OPT STRAP



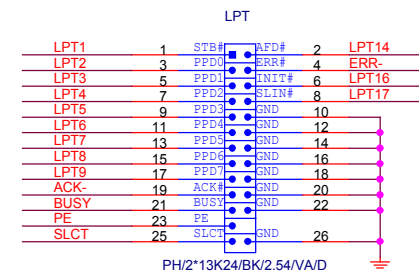
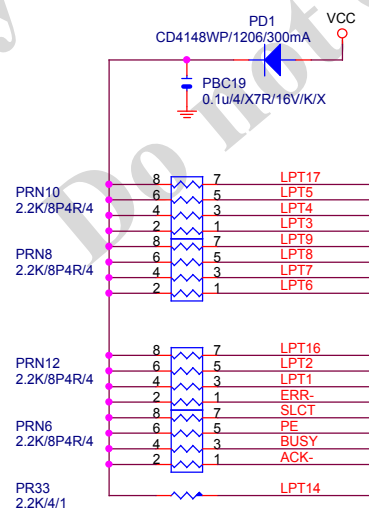
SIO 18V



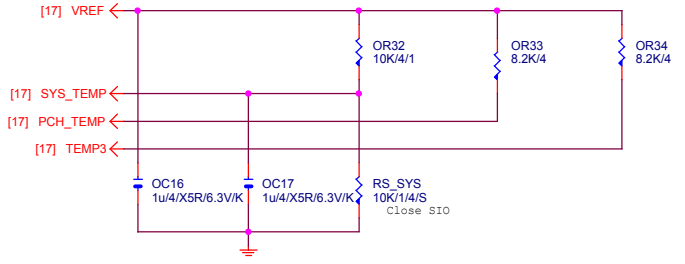
Gigabyte Technology			
Title PCH GPIO , CTRL , AUDIO			
Size C	Document Number GA-H81M-S2PV		Rev 3.0
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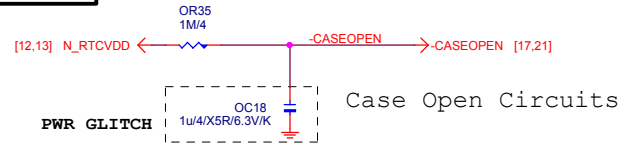
【技術通報R&D技術通報151】
33ohm Change to 68ohm



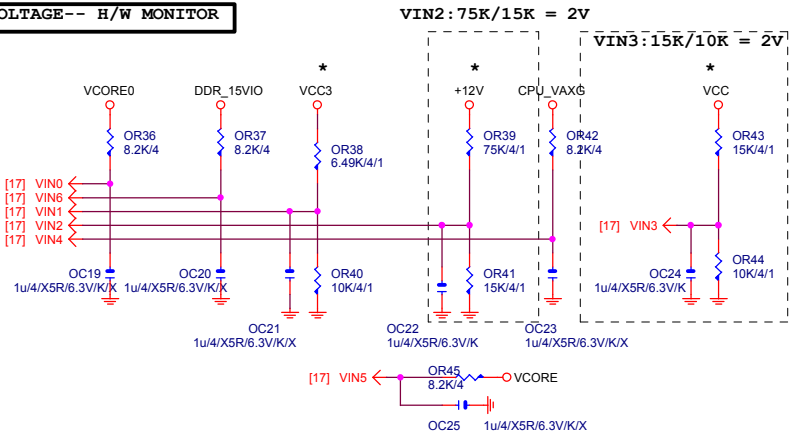
TEMP H/W MONITOR



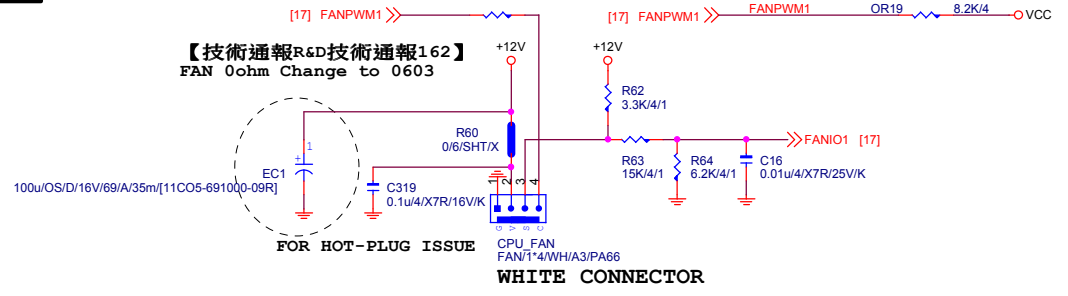
CASE OPEN



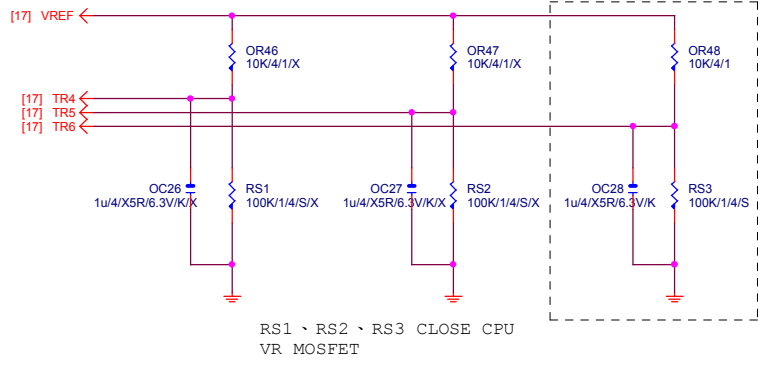
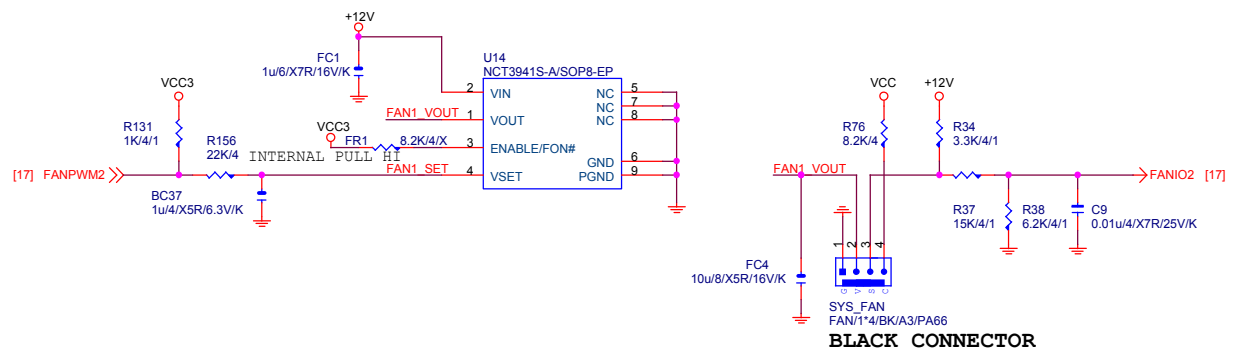
VOLTAGE-- H/W MONITOR

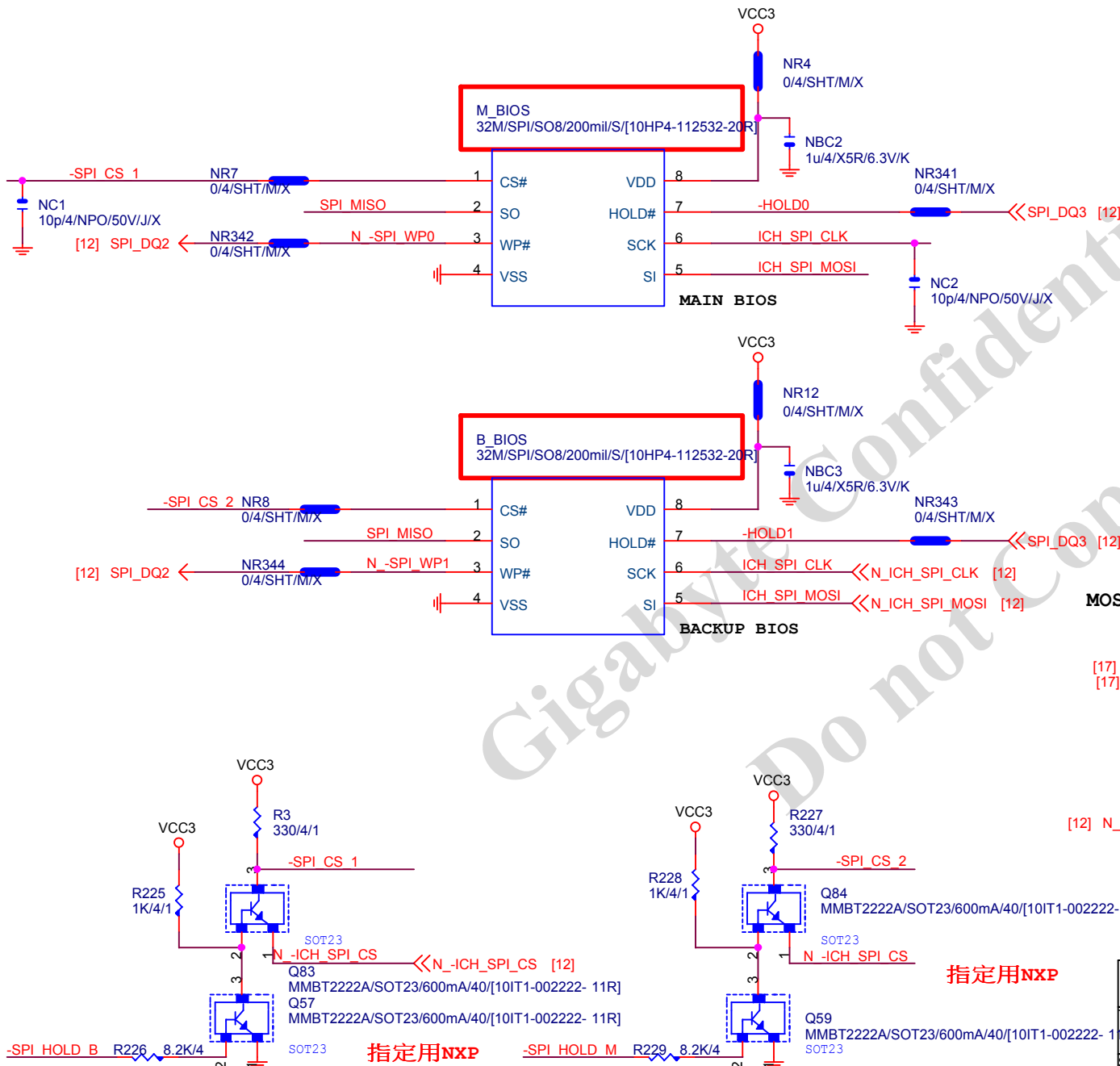


CPU SMART FAN



SYS SMART FAN

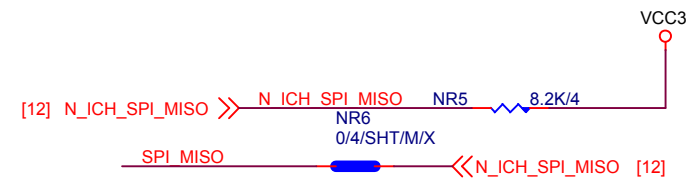
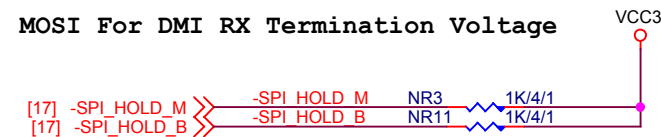




BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

MOSI For DMI RX Termination Voltage



Gigabyte Technology

DUAL BIOS

GA-H81M-S2PV

Rev
3.0

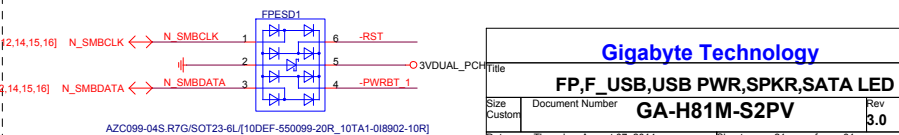
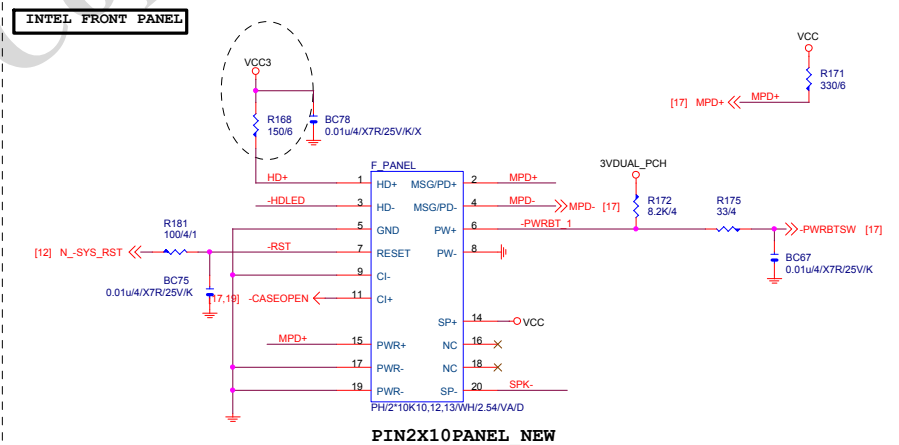
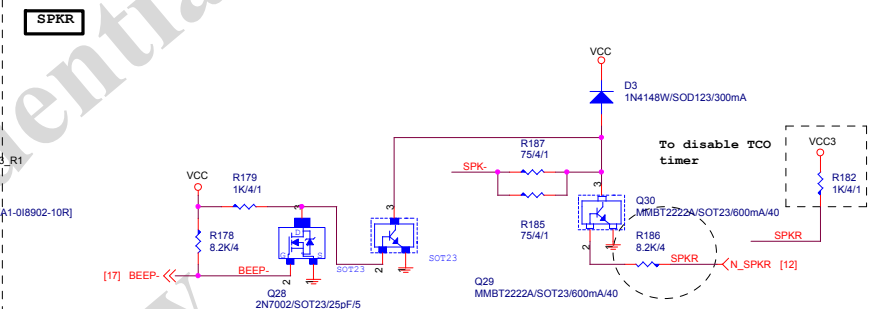
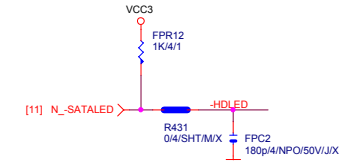
Title

Size Custom

Document Number

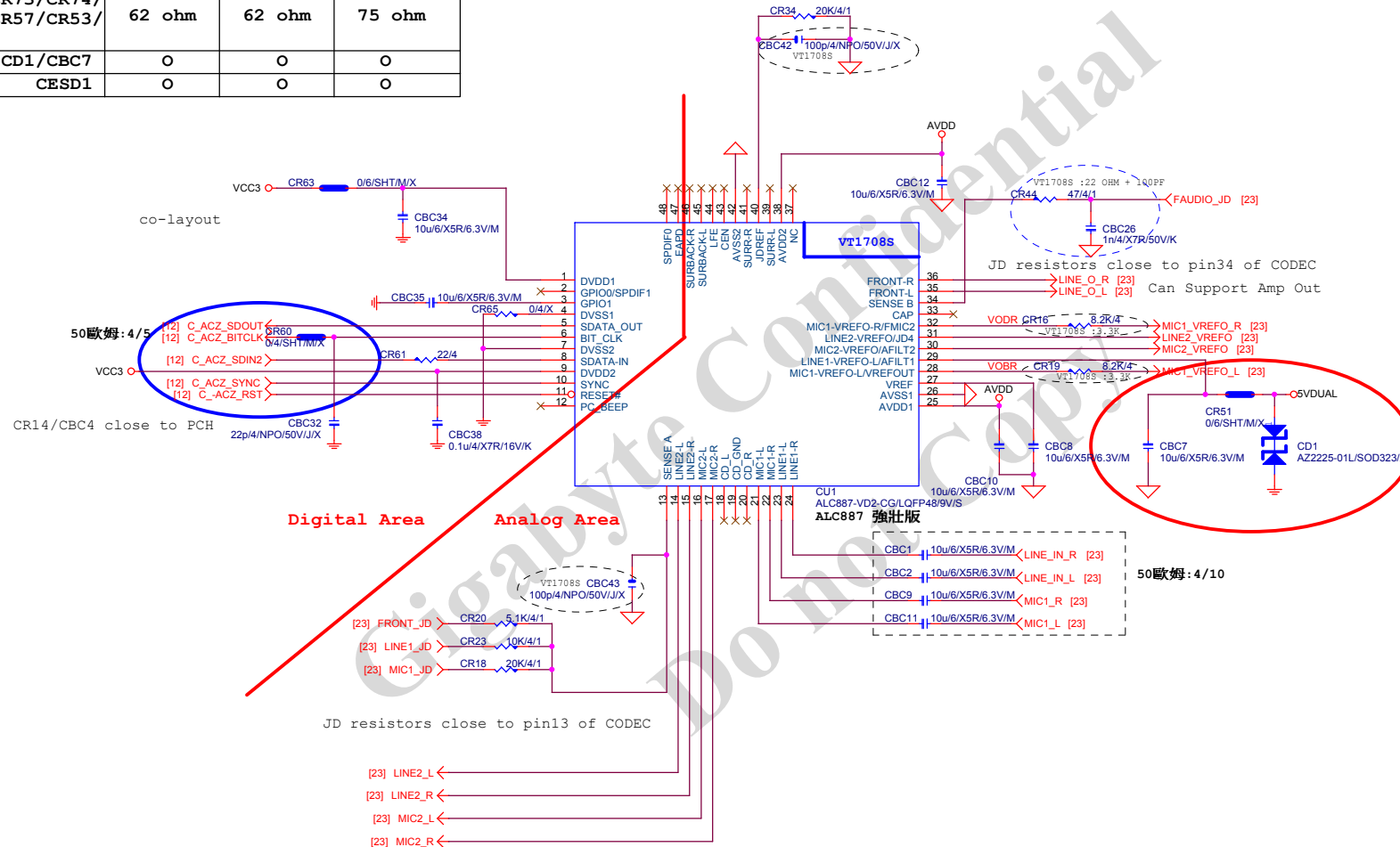
Date: Thursday, August 07, 2014

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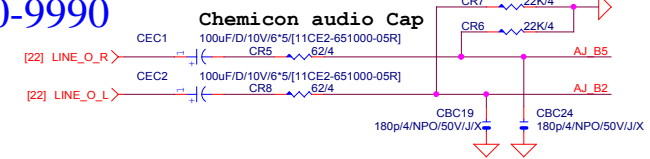


AZALIA CODEC *ALC892/ALC887-VD2/VT1708-CE Colay*

	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O



CONFIDENTIAL



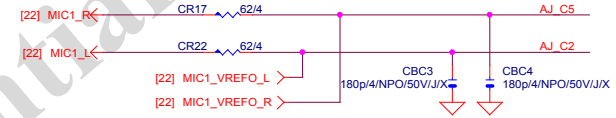
Only reserved for ALC888

LINE-IN

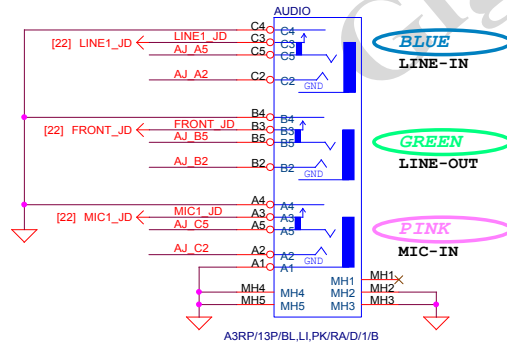
Verify MIC function in LINE-in

For 889A/888

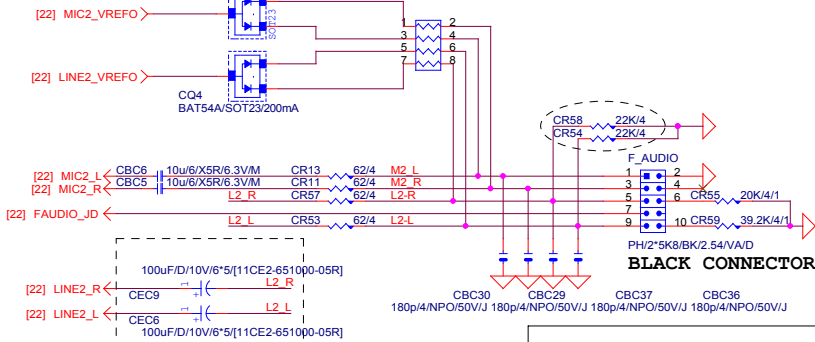
MIC-IN



SPDIF_OUT



AZALIA FRONT PANEL

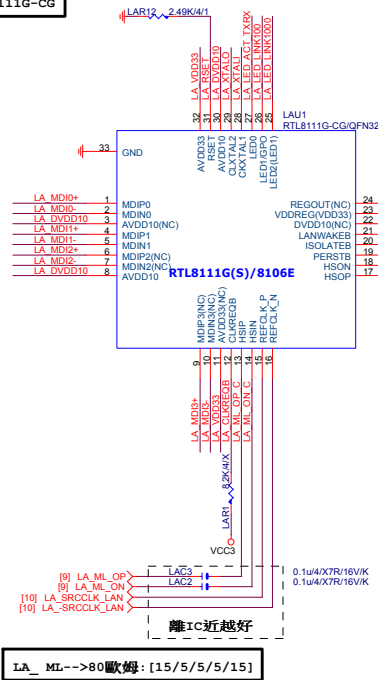


Chemicon audio Cap

Gigabyte Technology

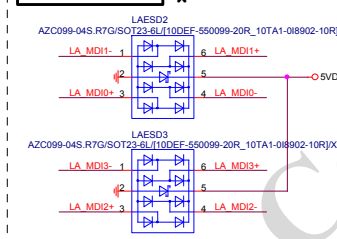
Title			
AUDIO JACK			
Size	Document Number	GA-H81M-S2PV	
Custom			Rev 3.0
Date:	Thursday, August 07, 2014	Sheet	23 of 31

LAN RTL8111G-CG

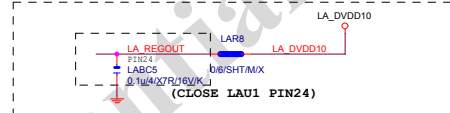
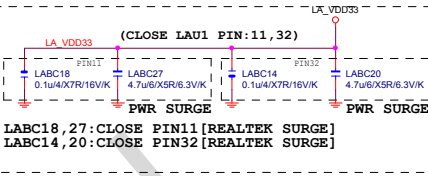
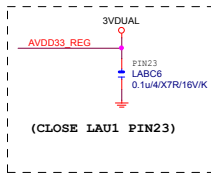
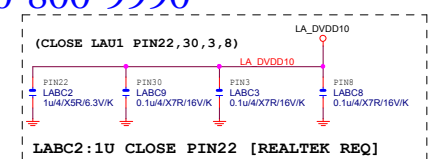


SRCCLK-->50歐姆: [18/4/10/4/18]

MDI ESD預留28KV *



LAN POWER

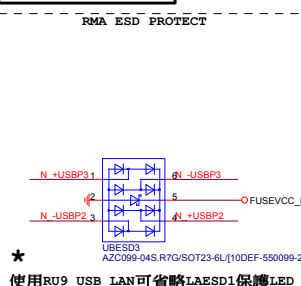


NOTE:
RT8106E: PIN3, 11, 22, 24-->NC
LABC2, LABC3, LABC5, LABC18, LABC27-->N/A

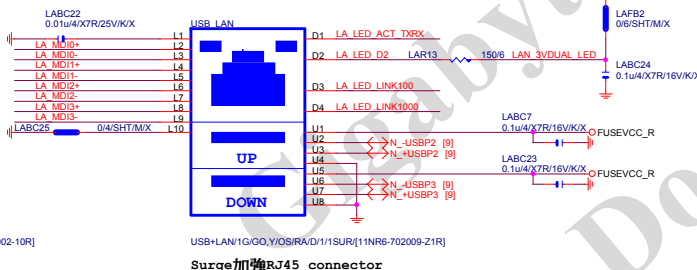
BOM NOTICE *

料號	規格	廠商
11NR6-702009-96R	1G LAN (12core)	UDE (RU9 ESD+)
[LED獨立走線, 可省略外加AZC099料件LAESD1]		
1. 9KV ESD BOM: USB LAN (RU9): 11NR6-702009-96R		
2. 28KV ESD BOM: USB LAN (RU9): 11NR6-702009-96R		
LAESD2, LAESD3: 上件AZC398-04S		

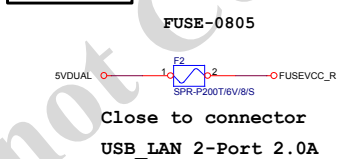
USB LAN CONNECTOR



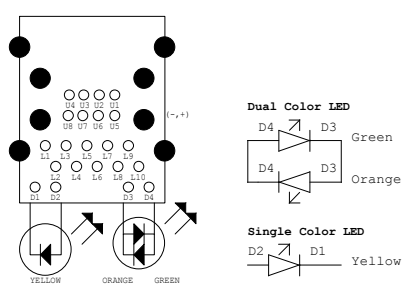
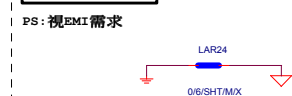
LA MDI-->100歐姆: [20/4/8/4/20]



USB POWER



EMI SHORT PAD



注意: USB PORT (目前: 暫代6, 7PORT)
USB-->90歐姆: [15/4.5/7.5/4.5/15]

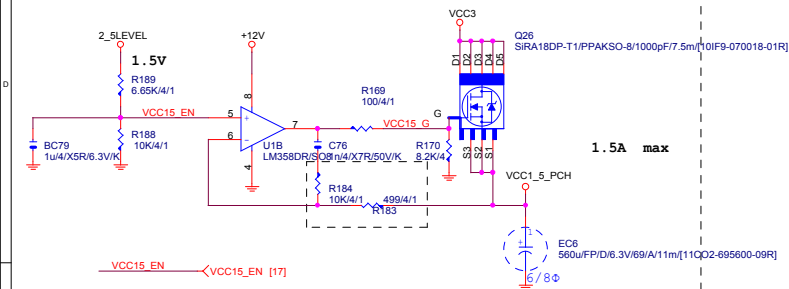
BOM NOTICE *

料號	規格	廠商
11NR6-702009-96R	1G LAN (12core)	UDE (RU9 ESD+)
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LAESD2, LAESD3: 上件AZC398-04S		

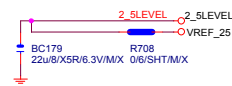
Gigabyte Technology

Title			Realtek RTL8111G
Size	Document Number	GA-H81M-S2PV	
Custom			Rev 3.0
Date:	Thursday, August 07, 2014	Sheet	24 of 31

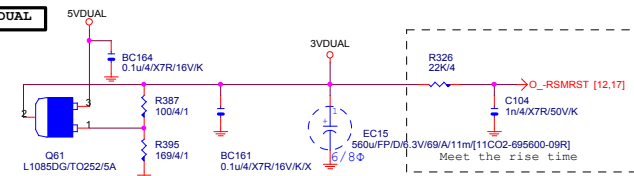
VCC1_5_PCH



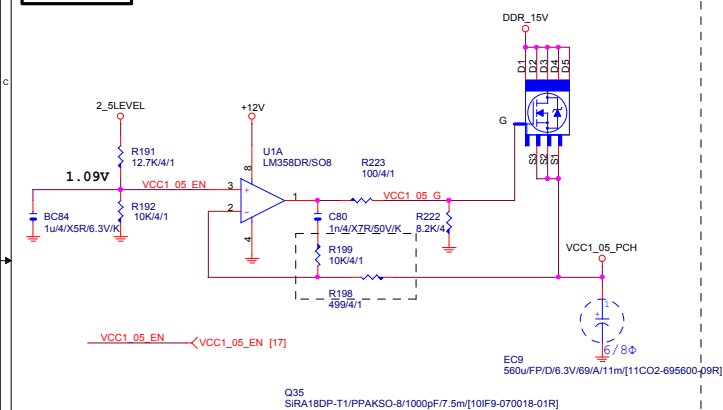
2_5LEVEL



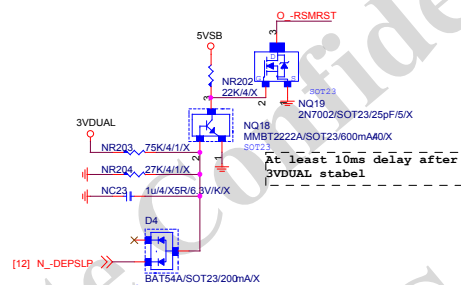
3VDUAL



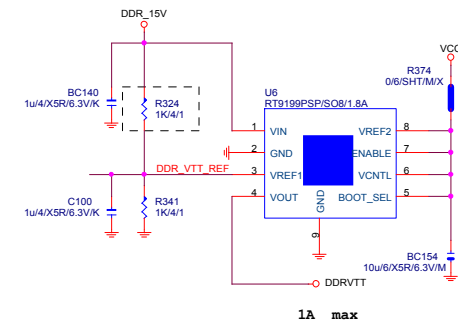
VCC1_05_PCH



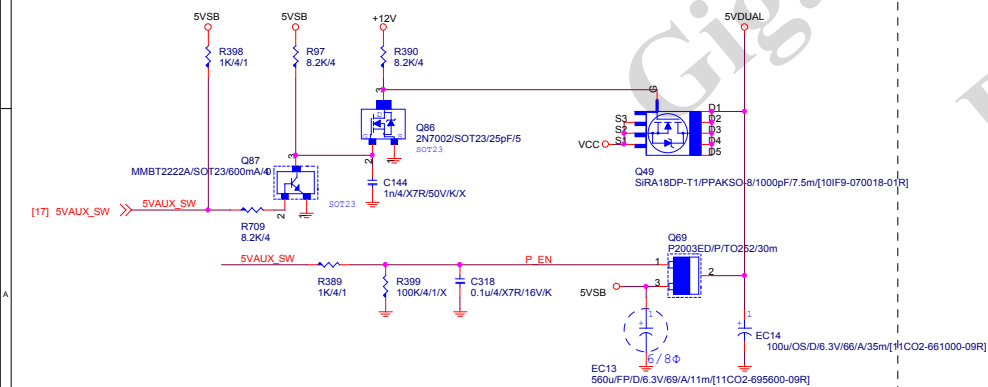
N/A



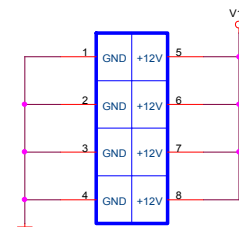
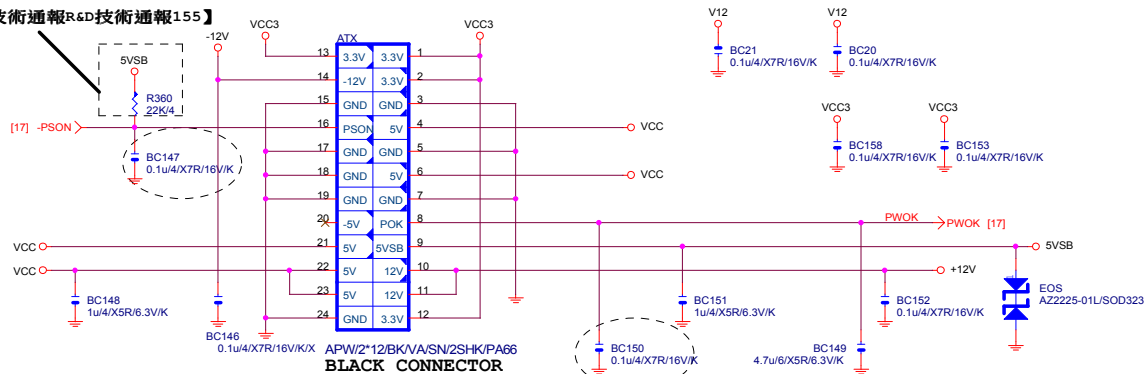
DDRVTT



5VDUAL



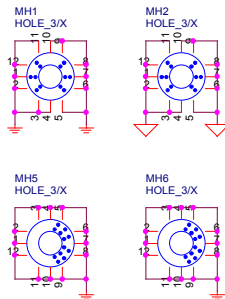
【技術通報R&D技術通報155】



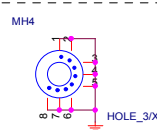
ATX_12V_2X4
APW/2*4/BK/OC/P/4.2/VA/SN/OH::Location ATX_12V_2X4

BLACK CONNECTOR

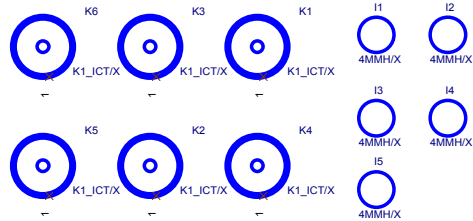
HOLE_4-RH-1



HOLE_4-RH-5MM-1



HOLE 4-RH-5MM-5PIN-1

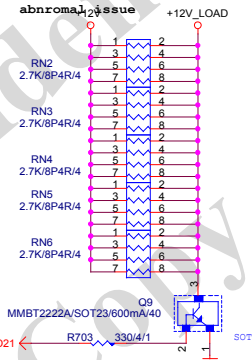


To prevent the 5VSB
under loading when
boot

HOLE 4-RH-5MM-1

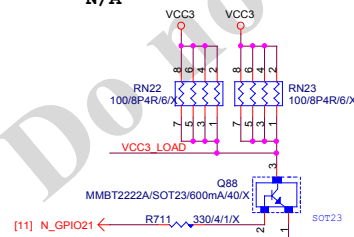
【技術通報R&D技術通報153】

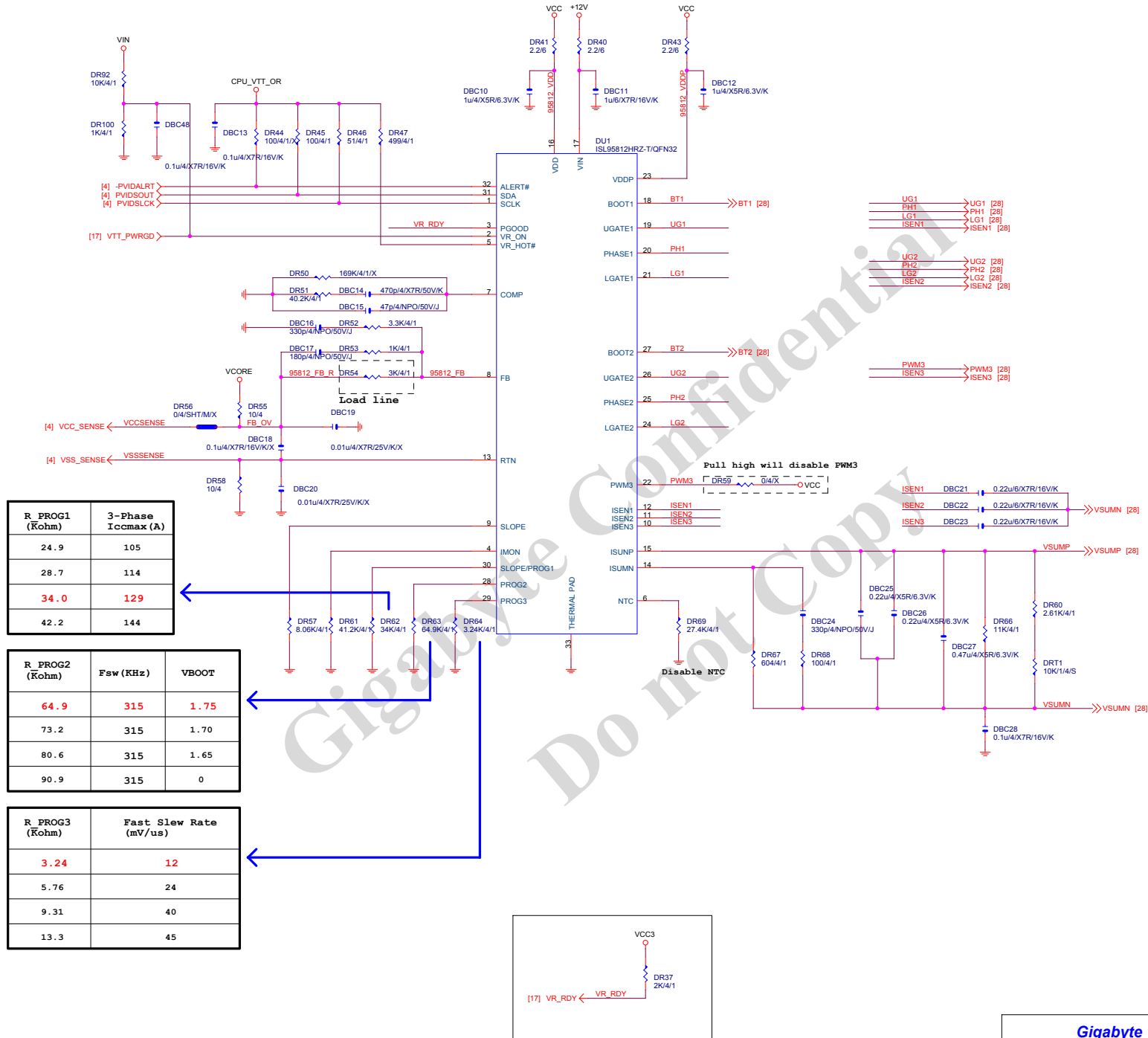
To fix 12V light load
abnromal issue +12V



FIX PWR MINMUN LOAD

N/A

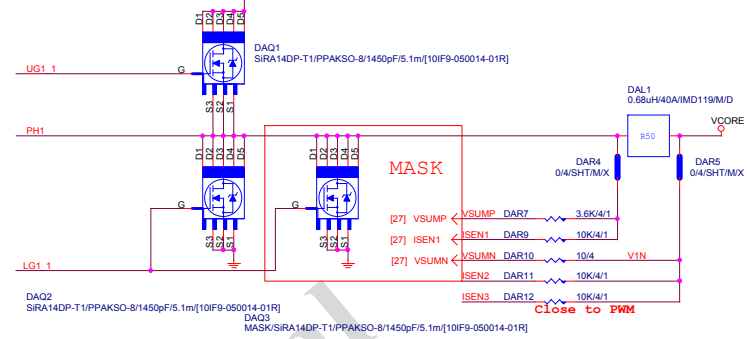
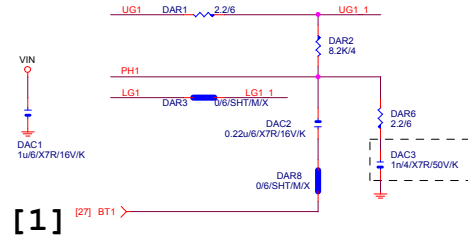




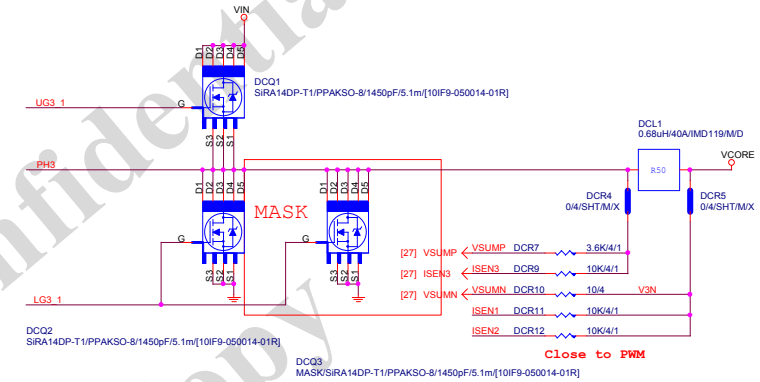
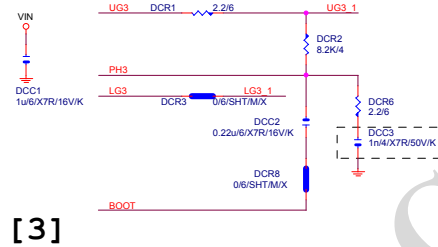
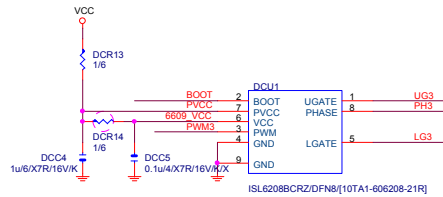
Gigabyte Technology

File			CPU CORE VR-1
Size	Document Number	GA-H81M-S2PV	
Custom			Rev 3.0
Date:	Thursday, August 07, 2014	Sheet 27 of 31	

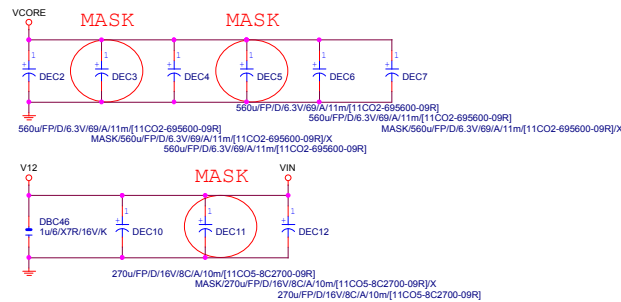
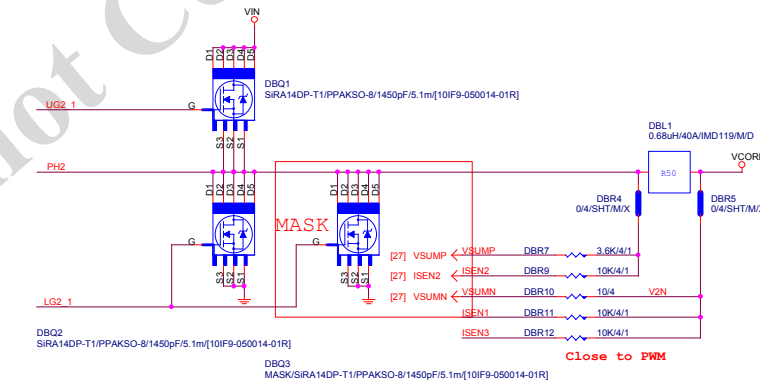
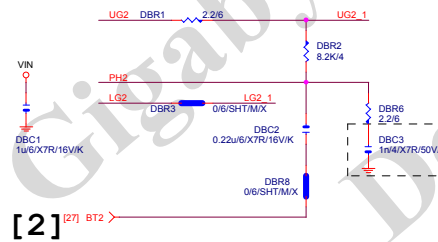
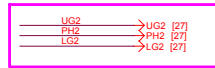
PHASE 1

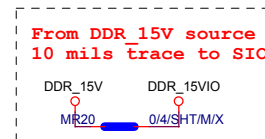


PHASE 3




PHASE 2



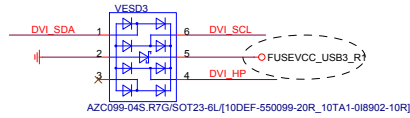
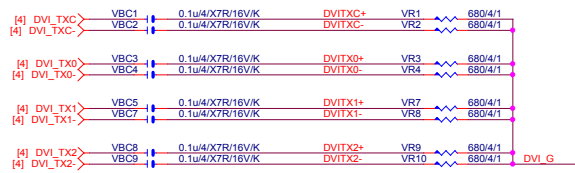


GP26	H	L	L	L
GP25	H	H	L	H
GP24	H	H	H	L
	1.35V	1.50V	1.65V	1.70V

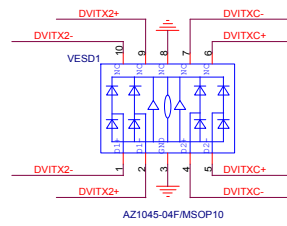
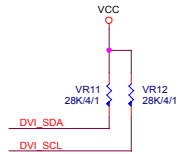
$$\begin{aligned} \text{Rocset} &= (\text{Iocp} * \text{Lgate}, \text{rdson}) / \text{Iocset} \\ \text{Rocset} &= (45\text{A} * 6.7\text{mOhm}) / 10\text{uA} = 30\text{K} \\ \text{Iocset} &= 10\text{uA} \end{aligned}$$

<div style="text-align: center;">  </div>			
Title			
DDR POWER			
Size	Document Number	GA-H81M-S2PV	Rev
Custom			3.0
Date:	Thursday, August 07, 2014	Sheet	29 of 31

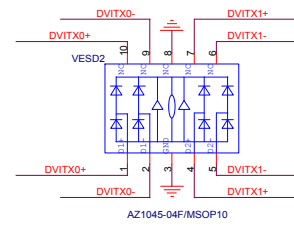
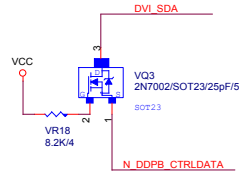
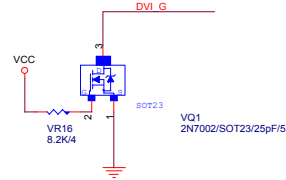
DVI



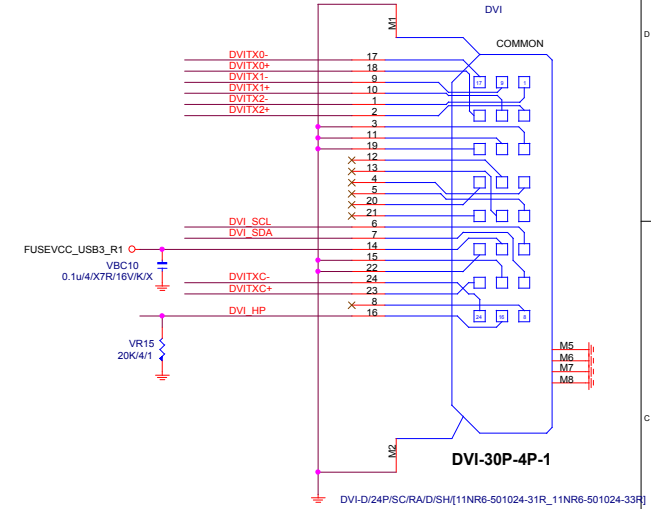
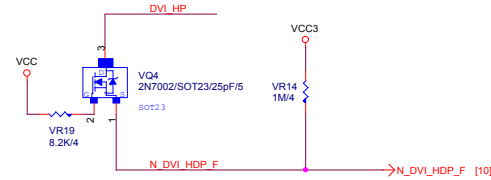
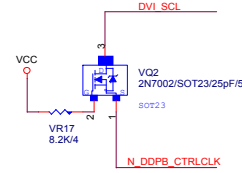
Close to connector



Close to connector



Close to connector



Gigabyte Technology

File			DVI
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PCIE TO PCI

PCI:5/4/5 Impedance=50 +- 15%

BA D[0..31] <-> BA_D[0..31] [16]

-BC BE0 <-> -BC BE0 [16]
 -BC BE1 <-> -BC BE1 [16]
 -BC BE2 <-> -BC BE2 [16]
 -BC BE3 <-> -BC BE3 [16]

-BPERR <-> -BPERR [16]
 -BSERR <-> -BSERR [16]

-BPAR <-> -BPAR [16]
 -BPOCK <-> -BPOCK [16]
 -BDEVSEL <-> -BDEVSEL [16]
 -BSTOP <-> -BSTOP [16]

-BTRDY <-> -BTRDY [16]
 -BIRDY <-> -BIRDY [16]
 -BFRAME <-> -BFRAME [16]

-PCIE_RST <-> -PCIE_RST [14,15,17]

-BPCIRST <-> -BPCIRST [16]

-BREQ0 <-> -BREQ0 [16]
 -BREQ1 <-> -BREQ1 [16]
 -BGNT0 <-> -BGNT0 [16]
 -BGNT1 <-> -BGNT1 [16]

-BPCIPME1 <-> -BPCIPME1 [16]



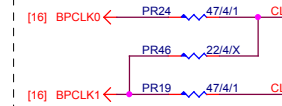
High: Enable PCI CLK 66MHz
 Low: Disable PCI CLK 66MHz



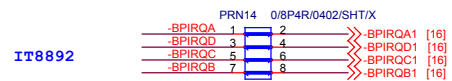
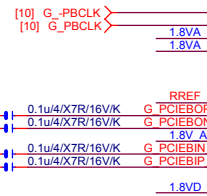
High: PCICLK INPUT form CLK Gen
 Low: PCICLK OUTPUT form IT8893 chip

Co-Lay IT8893 (IT8893 CLKOUT1 N/A)

IT8892: PR24 -> 47ohm
 IT8893: PR24 -> 22ohm



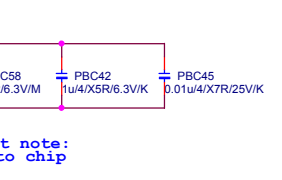
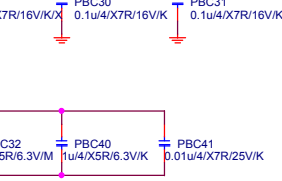
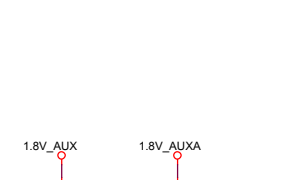
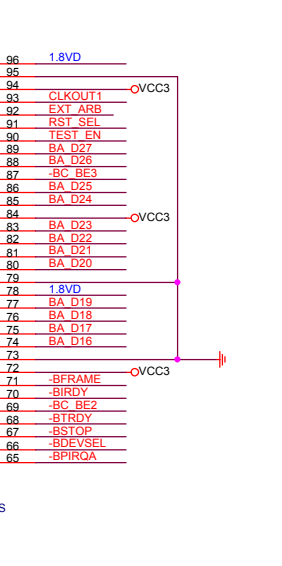
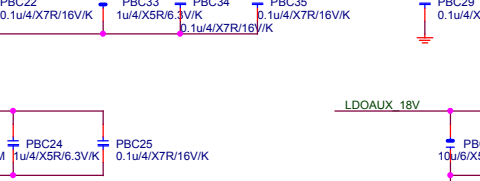
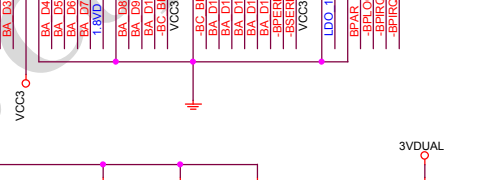
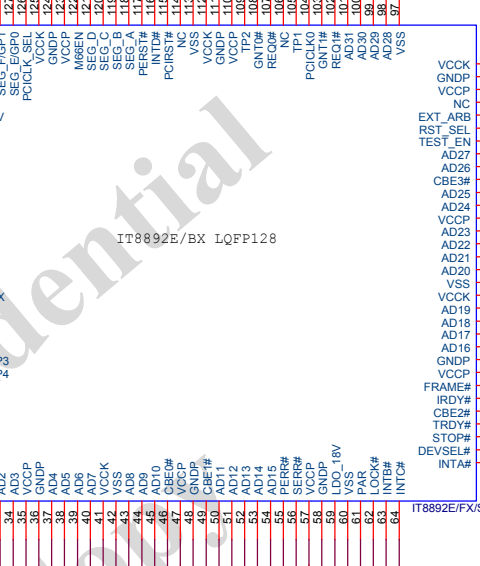
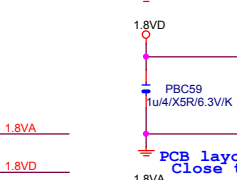
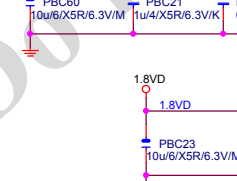
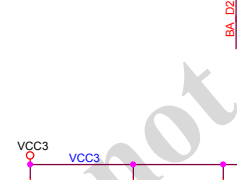
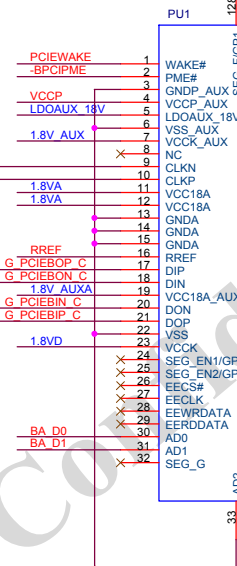
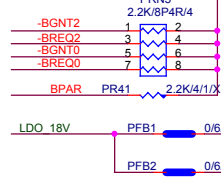
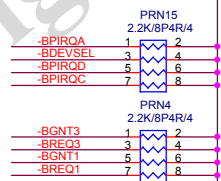
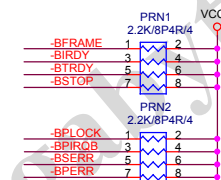
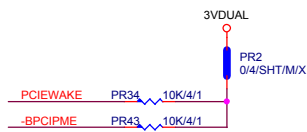
IT8892: PR19 -> O
 IT8893: PR19 -> X



PCI slot

PCI slot -BPCIPME1 PR27 <-> -N_PCIE_WAKE [12,14,15,24]

chipset side

PCB layout note:
Close to chip

Gigabyte Technology

Title		
ITE IT8892E		
GA-H81M-S2PV		
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